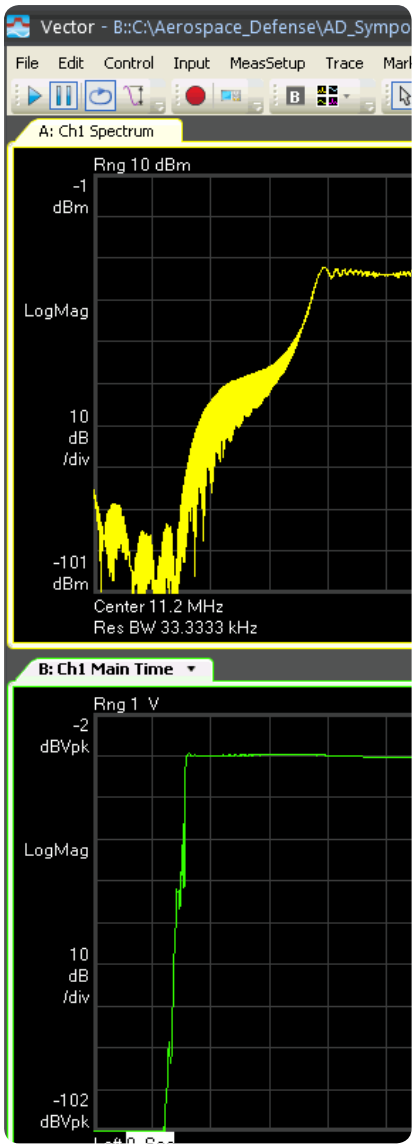
Mixed-Signal Integration Challenges in Complex Radar Systems

Application Note



Introduction

Radar design teams are today finding themselves at a crucial juncture. No longer can a radar design team focus solely on RF/microwave measurements when evaluating a prototype. More and more, the systems they design have become increasingly digital in nature, often employing field programmable gate arrays (FPGAs), digital signal processors (DSPs) along with radio frequency (RF) components to achieve the flexibility required to switch between different waveforms and configurations. This digital section requires a separate baseband designer or design team, and must be simulated and measured using tools that differ from those traditionally used by RF designers to debug, validate and characterize intermediate frequency (IF) and RF signals. Unfortunately, the disparate design and test methodologies used by the baseband design team designing the radar signal processor and RF team designing the RF exciters and receivers often result in a host of system integration issues and testing challenges.

This application note presents an alternate design and test approach for today's complex radar systems that relies on a common analysis platform to bridge the gap between baseband and RF designers and design teams. This approach uses the Agilent Vector Signal Analysis (VSA) software in conjunction with Agilent's logic analyzer and Infiniium Series Digital Oscilloscope. Agilent's SystemVue software is also used. By providing a common measurement framework, this approach makes it much easier for the baseband and RF teams to come together to create a working radar system.

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System-Level Integration Challenges

A conceptual block diagram for a complex radar system is shown in Figure 1. The digital baseband subsystem, or radar digital processor, may be implemented with a number of FPGAs and DSPs, and followed by a digital-to-analog (D/A) converter. The D/A converter outputs analog IF, which gets up converted to RF for the transmitter portion.

Traditionally, a tool such as a spectrum analyzer has been used to evaluate the IF and RF signals in radar systems. The baseband designer or design team must reconcile any issues with the RF design team. Because the baseband and RF design teams use different design and test methodologies, mixed-signal designs such as this radar transmitter subsystem can present significant challenges to the system engineer or system architect.

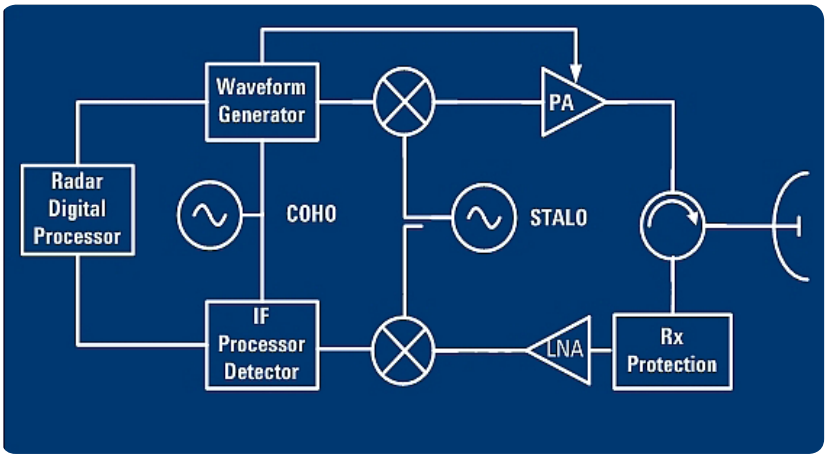

Figure 1. The radar digital processor can be comprised of FPGAs and DSPs and may be re-configurable for different functions.

Those challenges are largely related to the integration of the mixed-signal subsystems at the system level. When an issue is discovered at this late stage, it can be extremely difficult and time-consuming to determine its source. Waveform impairments, for example, can be an accumulation of mixed-signal impairments occurring in the FPGA implementation, D/A converter, IF/RF up-converter, and power amplifier. Making this determination can be difficult given that the system engineer has to deal with the disparate design and test methodologies of the digital and RF design teams. This problem serves to highlight the increasing need to use a common measurement approach to evaluate digital, analog, IF, and RF hardware.

A Common Measurement Approach

A common measurement platform offers a viable solution to this dilemma for complex radar design. One such platform is Agilent Technologies' 89600B Vector Signal Analysis (VSA) software. This advanced analysis solution provides simultaneous views of virtually every facet of complex wireless signals. Such information is critical to enabling engineers to achieve the clarity needed to find the root cause of signal problems.

The VSA software runs on a PC or inside PC-based instruments and measures over 70 signal standards and modulation types covering a range of applications (e.g., mobile communications, wireless connectivity, military communications, satellite communications, radar and more). Its advanced troubleshooting tools quantify spectral performance with high resolution FFT-based measurements; analyze time-domain signal quality; and characterize complex modulation down to the raw bits. The VSA works easily with spectrum analyzers, signal analyzers, oscilloscopes, logic analyzers, modular instrument systems, and simulation software. Because of this flexibility, engineers can evaluate signals anywhere in the block diagram including analog and digital baseband and IF, RF and microwave.

In the case of complex radar design where multiple tools are required to simulate and measure a design's digital portion, the VSA software is used in conjunction with Agilent's SystemVue software, logic analyzer and Infiniium Series Digital Oscilloscope (Figure 2). SystemVue, an open simulation and modeling environment, is used to create and simulate the radar design. VSA measurements on FPGA hardware or along the RF exciter/receiver chain (IQ, IF and RF) are performed with the logic analyzer (FPGA) or digital oscilloscope (IQ, IF and RF). This enables system engineers and architects to debug issues along the radar system's mixed-signal chain, while also helping to ensure the radar meets system-level requirements.

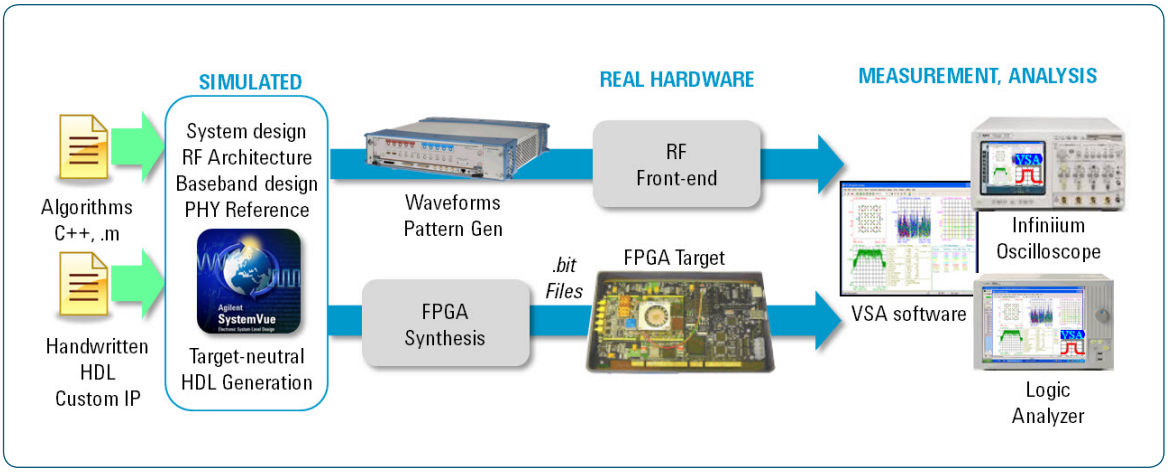

Figure 2. The process and tools shown here can be used for cross-domain model-based design (e.g., RF, communications and C++/HDL) of complex radar systems. The process results in a FPGA implementation in real hardware, where measurements can be taken via a logic analyzer and Infiniium Series oscilloscope.

The logic analyzer works with FPGA design tools to automatically capture the design's internal digital signals at stages across the baseband. Captured digital data can be processed with the VSA software for advanced analysis. Once the digital signals are converted into analog IQ or IF with a D/A converter(s), the Infiniium Series oscilloscope captures and analyzes the waveforms with the VSA software again. Running on the oscilloscope, the VSA software allows designers to evaluate waveform characteristics in the analog IQ/IF/RF domains.

Using the VSA software as a common analysis platform has a number of significant benefits; namely, that it bridges the gap between digital and RF subsystems by allowing the baseband and RF design teams to more closely work together using the same set of tools. The result is faster, easier debug and validation. Using the VSA software on both the logic analyzer and digital oscilloscope, for example, designers can probe the mixed-signal chain to isolate issues and gain insight into where waveform impairments are occurring. Consequently, having an identical analysis engine in both the digital and analog/RF domains provides designers with a powerful cross-domain analysis tool that gives them greater insight into their radar system's mixed-signal performance—whether it's digital baseband, analog IQ/IF/RF or both. This greater insight helps significantly reduce the challenges associated with system integration.

Using SystemVue to Create and Simulate a Radar Design

To better understand how the VSA can serve as a common measurement platform for complex radar design, consider a fixed-point baseband design to generate a linear frequency modulation (LFM) chirped radar (Figure 1). Chirped radar utilizes a type of pulse compression in which the frequency modulation happens in a linear fashion across the pulse width. Pulse compression is often applied in a radar system to extend range and increase resolution. Essentially, the pulse gets frequency modulated, which in turns causes each part of the pulse to have a unique frequency. This means that reflections from a target, which normally might have had overlapping return signals in the frequency domain, can now be more easily and completely separated due to the unique frequency components at hand.

In this example, the LFM chirped radar waveform is implemented with fixed-point models that generate HDL code for an FPGA implementation (Figure 3). SystemVue software is used to create and implement the chirp radar design using the process in Figure 2.

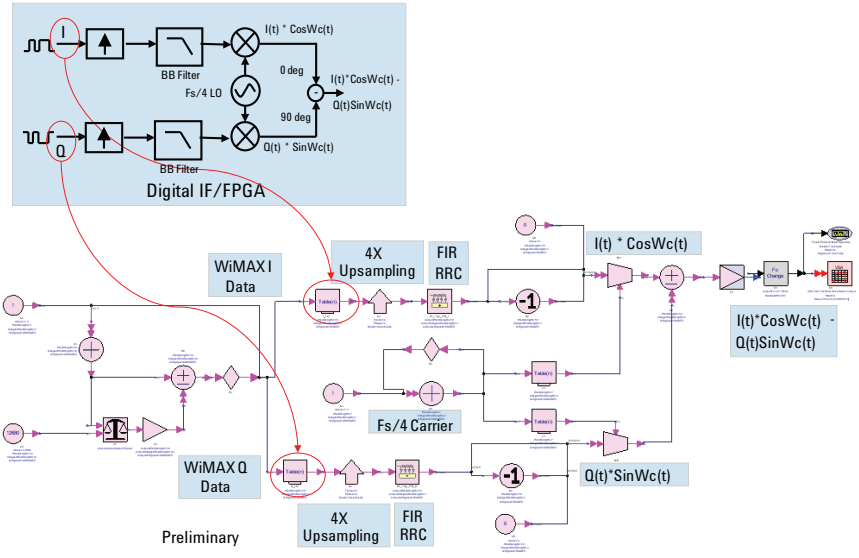

Figure 3. Shown here is the chirp radar baseband section with digital IQ and digital IF sections.

The SystemVue simulator is used to model a fixed-point IQ modulator design consisting of radar LFM I and Q data stored in a lookup table. The I and Q waveforms are then upsampled by a factor of four, root-raised cosine filtered and digitally multiplexed onto a digital IF carrier centered at Fs/4. Next, the digital IF is converted to an analog IF using a D/A converter.

The VSA software is used in simulation to evaluate the fixed-point design during the design phase. It will also be used during a later phase to test the FPGA with the logic analyzer. Hardware description language (HDL) code is generated from the fixed-point models in SystemVue. This code is used to implement the design with an FPGA, in this case, a Xilinx Virtex-4 FPGA development board. The resulting hardware will be measured using a logic analyzer and oscilloscope, using the VSA software in both instruments.

Accessing Digital Signals

Now that the chirp radar design has been created and simulated, the next step is to insert test points so that the digital signals can be accessed. This can be accomplished using the setup in Figure 4. In this setup, the FPGA development board is probed using an Agilent logic analyzer with its FPGA dynamic probe capability. This capability allows designers to select various internal FPGA signal banks to evaluate their design with the VSA software at various probe points in the implementation.

Note that when running on the logic analyzer, the VSA software is used to evaluate the modulation characteristics of the digital radar waveform. When running on the Infiniium Series oscilloscope, the VSA software measures the analog IF signal converted from the digital IF signal by the D/A converter on the FPGA output. This enables the system engineer to evaluate the radar waveform characteristics in the digital domain (via the logic analyzer) or the analog IQ/IF/RF domain (via the oscilloscope or an RF signal analyzer).

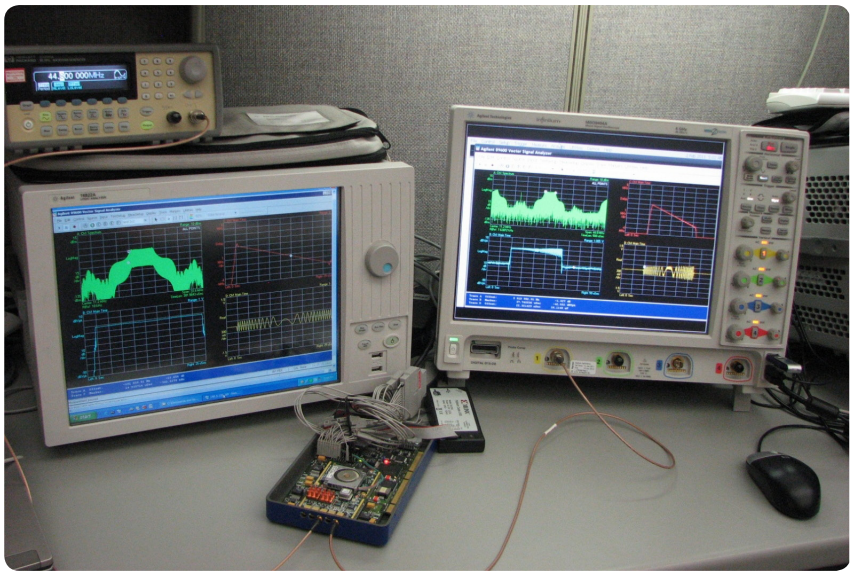

Figure 4. With this setup, the logic analyzer on the left probes internal FPGA points, while the Infiniium Series oscilloscope on the right probes the D/A output analog IF. Both instruments are running the VSA software.

Using the test setup in Figure 4, signals are probed along various stages of the FPGA implementation such as the filtered I/Q or digital IF signals data captured. Signals are picked up with a switching multiplexer (MUX) measurement core located inside the Virtex-4 FPGA development board. The probe points are defined using the ChipScope Pro Core Inserter application from Xilinx (Figure 5). With this application, designers can define the type of measurement core (state or timing), number of signal banks, how many pins will be used for debug signals, and exactly what FPGA I/O pins will be used to bring out debug signals.

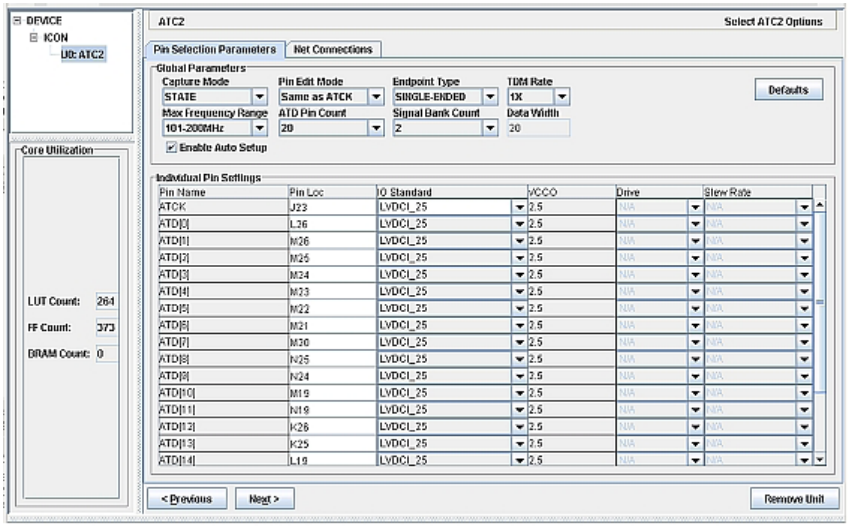

Figure 5. The Xilinx ChipScope Pro measurement core definition interface allows designers to define probe points.

FPGA nets are probed at the upconverted and filtered I and Q signal level, as well as at the digital IF output that drives the input to the D/A converter. The logic analyzer's FPGA dynamic probe capability then works with the FPGA measurement core to enable designers to make meaningful measurements. Using it, designers can select another measurement bank, in this case, the digital IF signal just prior to the I/O ring of the FPGA. This signal goes out of the FPGA I/O and is routed to the D/A converter input on the PC board.

To trace signals of interest, the Xilinx Plan Ahead FPGA design interface tool is utilized. Suppose, for example, that the designer wanted to probe the digital IF signal just inside the I/O ring of the FPGA, prior to driving the D/A converter. Figure 6 shows a graphical view of the FPGA implementation within Plan Ahead with the design's output signals defined. By double-clicking on one of the signals from the bus DAC1_D_OBuf, a schematic block diagram window opens that shows the FPGA nets associated with this bus. Double-clicking on one of these nets enables the tool to trace the signal back to the previous stage. By repeating this process, signals can be traced back to a specific point-of-interest for probing.

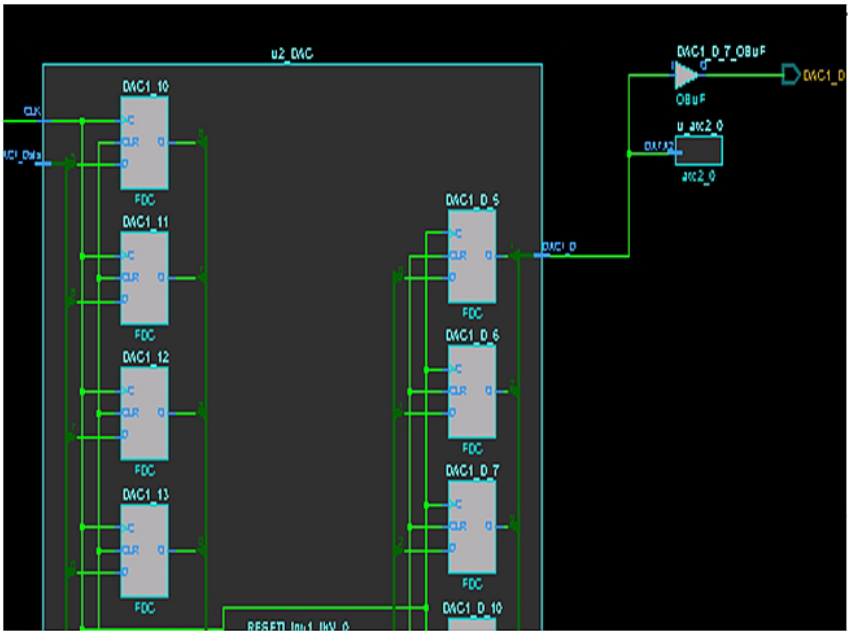

Figure 6. This schematic view shows the FPGA's DAC input signals in the Xilinx Plan Ahead tool.

In this case, FPGA nets of interest are chosen from inside ChipScope Pro Core Inserter. The designer simply searches for the net names of interest and then designates those nets to signal banks. The digital IF signals were found by looking into the hierarchy of the 'Structure/Nets" window, highlighted, and then the 'Make Connections' button pressed to associate those signals to a particular signal bank. The same thing was done for the digital I and Q signals for a second signal bank.

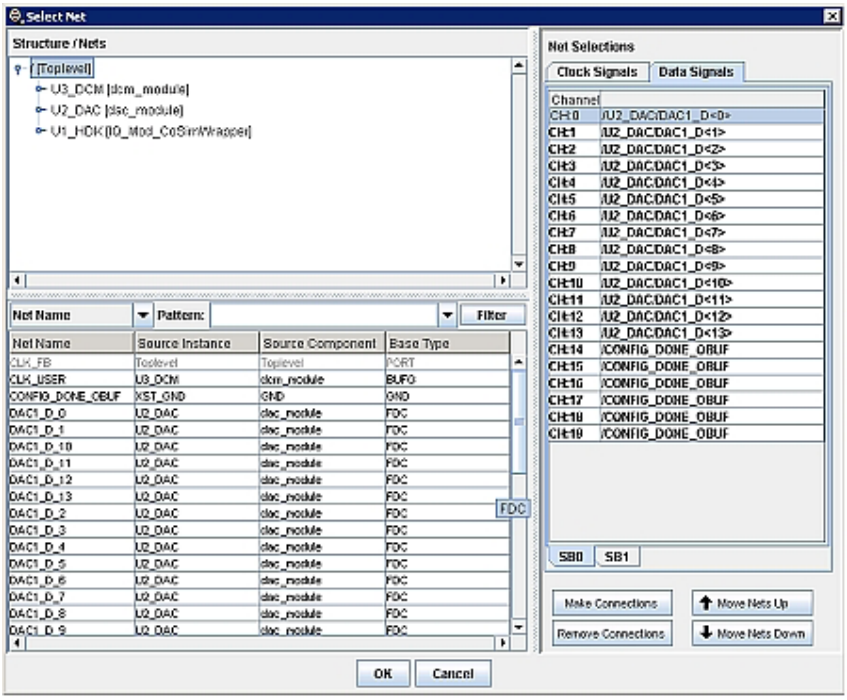

Figure 7. In this menu, the ChipScope Pro Core Inserter assigns DAC inputs to Signal Bank 1.

Gaining Insight Into The Design

Now that test points have been inserted, designers can glean insight into the design by making measurements on the logic analyzer, a process greatly simplified by the analyzer's FPGA probing capability. Analysis is performed with the VSA 89601B software.

The programming .bit file for the FPGA design is downloaded into the FPGA directly from the logic analyzer interface via a JTAG connection (Figure 8). The designer then imports bus signal names from the .cdc file created by the ChipScope Pro Core Inserter application when probing points were chosen. Next, automatic pin mapping occurs. With this process, debug signals on the output pins of the FPGA are discovered and automatically mapped to the logic analyzer input channels.

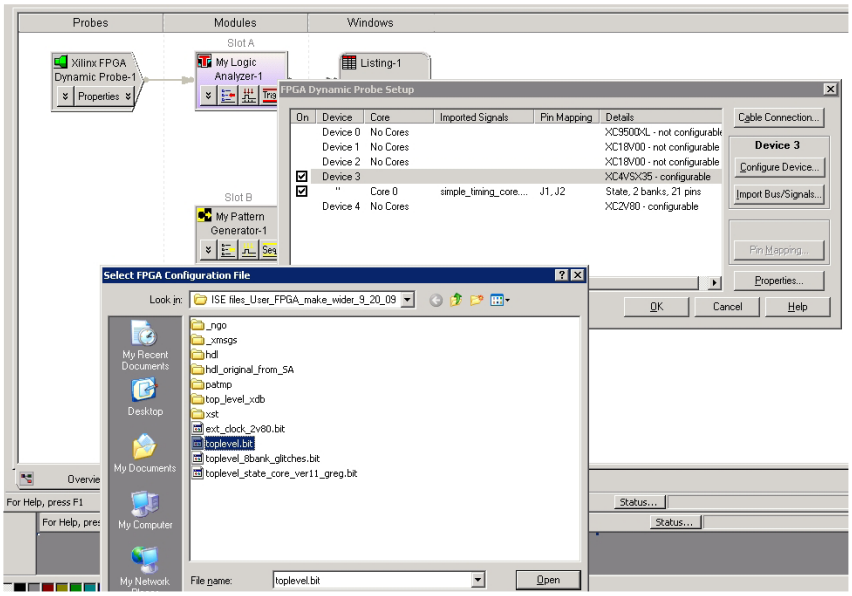

Figure 8. The process of configuring the FPGA with instrumented design is illustrated here.

At this point, a trace can be taken with the logic analyzer. To do this, the logic analyzer is set up such that the proper clock input is defined and threshold levels are set to match the FPGA output voltage levels. The logic analyzer's capture mode is also set to match the FPGA debug signal output. An option to use time-division multiplexing enables the designer to get two nets out simultaneously in real time per each FPGA pin. Once the set up is complete, the designer simply selects the signal bank to look at (Figure 9). Figure 10 shows the logic analyzer capture of the DAC input digital signal, or trace.

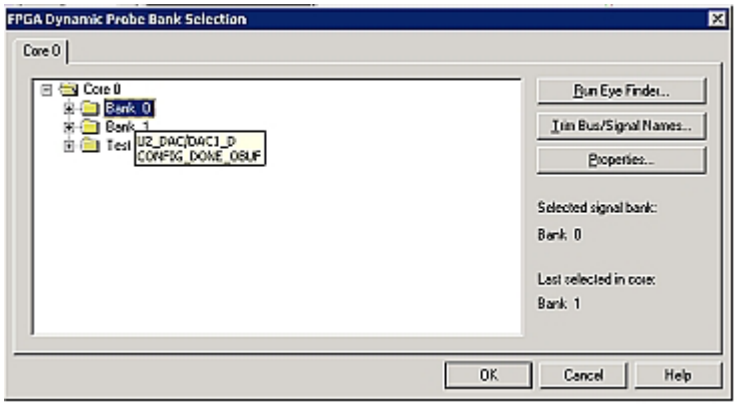

Figure 9. This menu is used to select the DAC input signal bank.

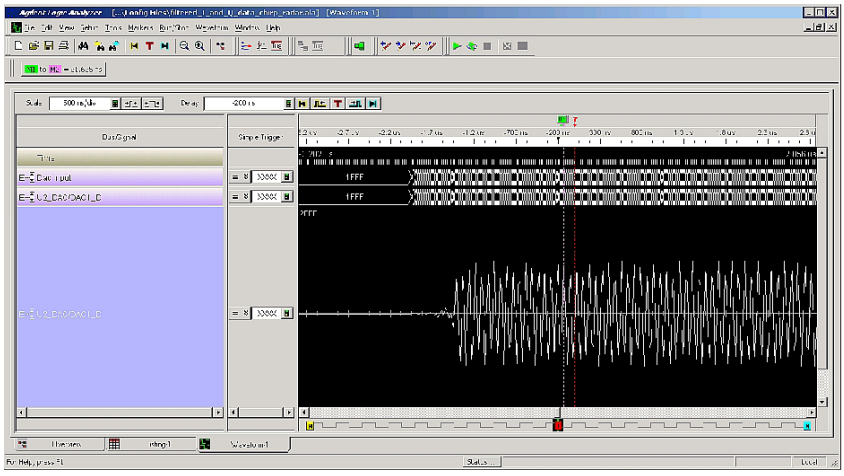

Figure 10. This trace results from the logic analyzer capture of digital IF signals before the FPGA I/O ring.

The digital IF waveform captured by the logic analyzer can now be imported into the VSA software for analysis (Figure 11). Various settings in the VSA's Input Property dialog box (e.g., sample rate and center frequency) simplify this process.

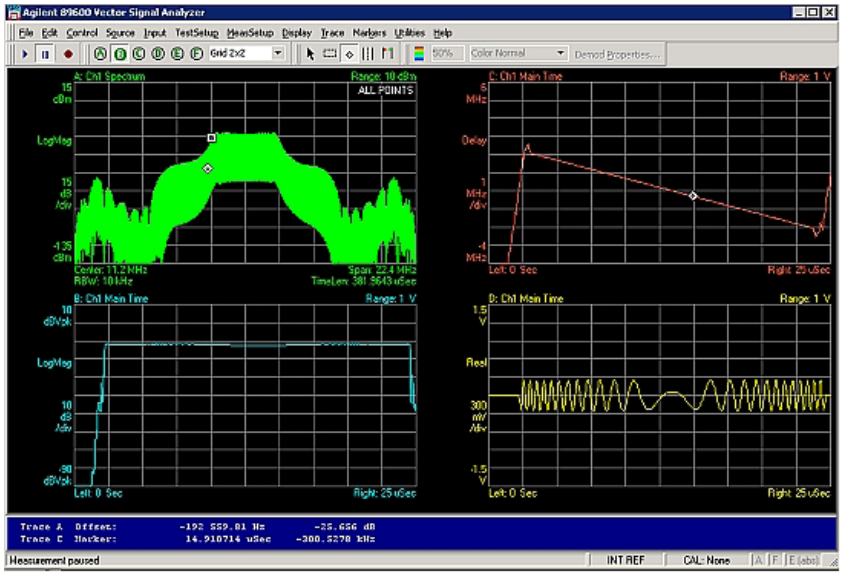

Figure 11. In this VSA screenshot, the radar spectrum is shown in the upper left, the log magnitude of the radar pulse is shown on the lower left, the chirped frequency across the width of the pulse is shown on the upper right, and the real or in-phase (I) component of the waveform is shown on the lower right.

Finally, the digital IF signal that the baseband team is working with can be compared to the analog signal that the analog/RF team is working with. First though, the analog IF signal must be measured. To do this, the DAC output signal is measured with the real-time digital Infiniium Series oscilloscope (Figure 12). This analog signal can be analyzed by the VSA software as well.

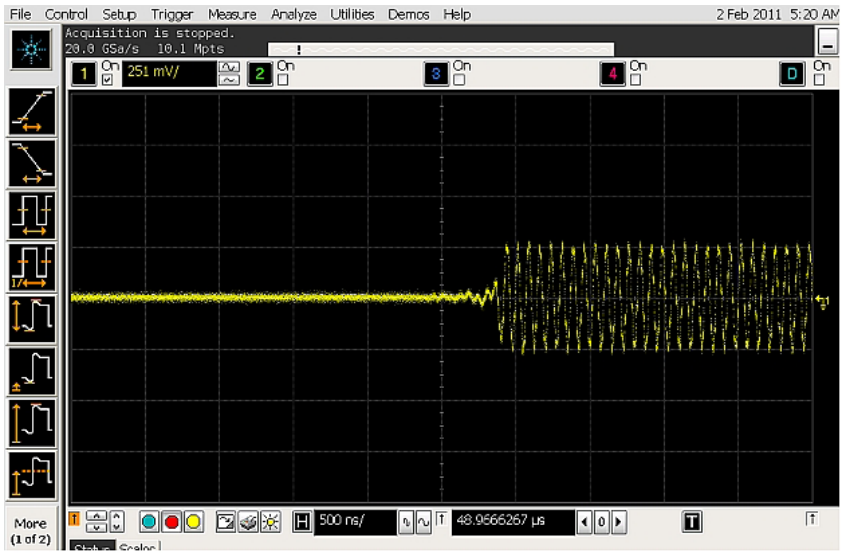

Figure 12. The chirp radar signal on the output of the D/A converter can be captured with a real-time digital oscilloscope. The oscilloscope is connected via a coax cable to a connector on the platform. This analog signal is analyzed with the VSA software.

As shown in Figure 13, the VSA software presents useful information about this IF signal. Notice that when the system is operating properly, a very similar set of data appears in each VSA display corresponding to the digital IF and the analog IF signals. By providing a consistent display across digital, IF and RF domains, designers can probe the signal in the FPGA implementation at various points, or anywhere along the analog IQ/IF/RF signal path. This side-by-side analysis can be very useful when an undesired waveform impairment is seen along the path. In this case, the designer can trace the signal back in the signal path to find the root cause of the problem.

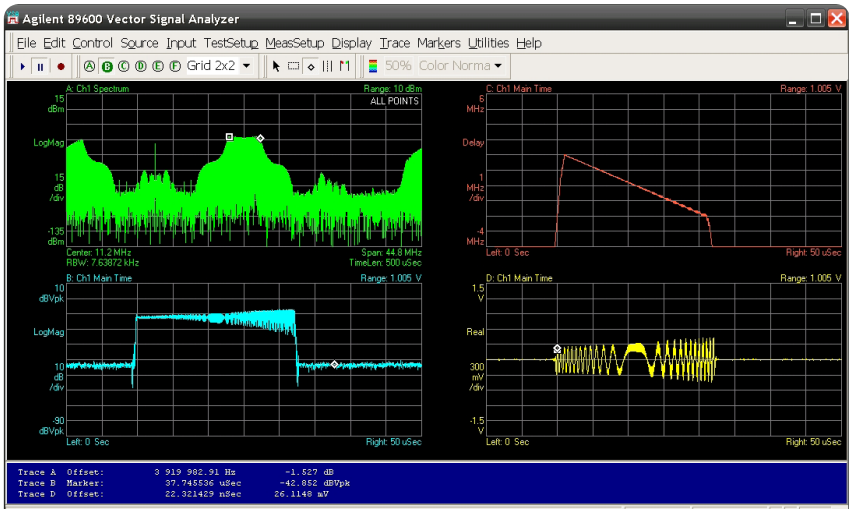

Figure 13. The analog IF signal from the DAC output is analyzed by the oscilloscope and VSA software.

Dealing with Issues

When the digital IF waveform in one VSA display screen does not match the analog waveform in another VSA display screen, the designer can utilize digital probe points placed along the baseband signal path to assist in debugging and validation efforts. The logic analyzer's FPGA probing tool plays a critical role here. Using this application, the designer can switch to another test point, namely the other signal bank for the filtered digital I and Q data. The MUX measurement core uses the routing fabric of the FPGA to "touch" those nets, bringing them out for the logic analyzer to capture. The FPGA dynamic probe then automatically sets up new bus names on the logic analyzer and subsequently, displays the new signal busses and/or signals (Figure 14).

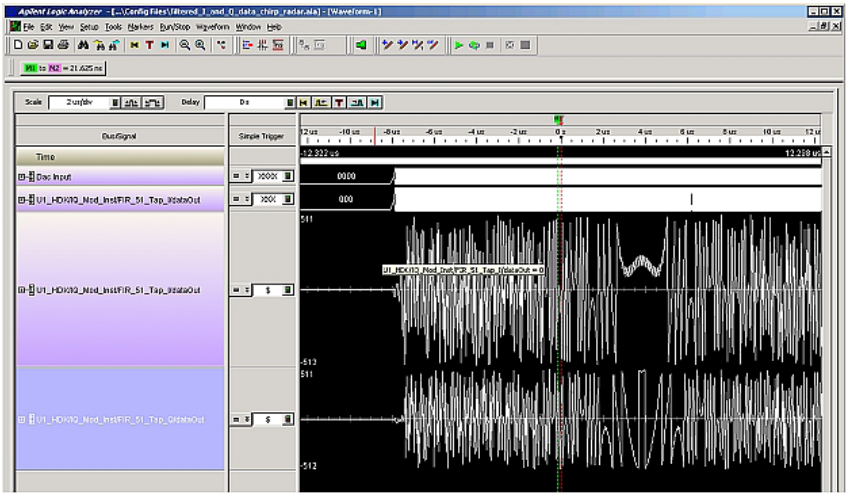

Figure 14. Shown here is the classic time-domain view of the I and Q vector modulation signals for a chirp radar as captured on the logic analyzer and displayed in the "chart" mode.

The important point to note here is that with VSA software, designers gain access to and can consistently measure and display digital, IQ, IF, and RF waveforms. When inconsistencies are found, a probing application such as that available in Agilent's logic analyzer can be utilized to isolate problems and identify their root cause.

Conclusion

The mixed-signal integration challenges inherent in today's complex radar systems demand a new approach to system-level testing. It requires an approach that employs a common measurement platform to bridge the gap between the baseband and RF design teams and their respective design and test methodologies. Agilent's 89601B VSA software provides the ideal solution to this dilemma, working easily with oscilloscopes, logic analyzers and simulation software, among other instruments. Using the VSA software with these other solutions, baseband and analog/RF teams can now better work together to identify the root cause of problems in their design. Having an identical analysis engine such as VSA essentially normalizes the acquired information in each domain such that these diverse engineering teams have a common connection point for analysis. Engineers can therefore, evaluate signals anywhere in the block diagram including analog and digital baseband and IF, RF and microwave, gaining greater insight into their complex radar design and minimizing system integration risks.

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